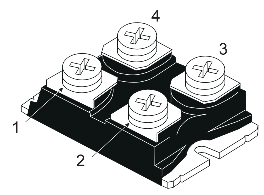
# STE70NM50

## N-CHANNEL 500V - 0.045Ω - 70A ISOTOP
## Zener-Protected MDmesh™Power MOSFET

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STE70NM50 | 500V | < 0.05Ω | 70 A |

- TYPICAL $R_{DS}$(on) = 0.045Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE




**ISOTOP**

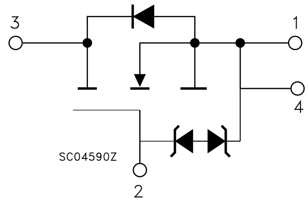
### DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

**INTERNAL SCHEMATIC DIAGRAM**




### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 500 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 500 | V |
| $V_{GS}$ | Gate- source Voltage | ±30 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C | 70 | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 44 | A |
| $I_{DM}$ (•) | Drain Current (pulsed) | 280 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 600 | W |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C=100pF, R=15KΩ) | 6 | KV |
| | Derating Factor | 5 | W/°C |
| dv/dt (1) | Peak Diode Recovery voltage slope | 15 | V/ns |
| $T_{stg}$ | Storage Temperature | –65 to 150 | °C |
| $T_j$ | Max. Operating Junction Temperature | 150 | °C |

(•)Pulse width limited by safe operating area

(1)$I_{SD}$ ≤60A, di/dt ≤400A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_j$ ≤ $T_{JMAX}$

### THERMAL DATA

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 0.2 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 30 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | 300 | °C |

### AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 30 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 35 V) | 1.4 | J |

### ELECTRICAL CHARACTERISTICS ($T_{CASE}$ = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 500 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating | | | 10 | µA |
| | | $V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20V | | | ± 10 | µA |

ON (1)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$, $I_D$ = 250µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10V, $I_D$ = 30A | | 0.045 | 0.05 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D$ = 30A | | 35 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | | 7500 | | pF |
| $C_{oss}$ | Output Capacitance | | | 980 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 200 | | pF |
| $R_G$ | Gate Input Resistance | f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain | | 1.5 | | Ω |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on Delay Time<br>Rise Time | $V_{DD}$ = 250V, $I_D$ = 30A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10V<br>(see test circuit, Figure 3) | | 51<br>58 | | ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 400V, $I_D$ = 60A,<br>$V_{GS}$ = 10V | | 190<br>53<br>97 | 266 | nC<br>nC<br>nC |

SWITCHING OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{r(Voff)}$<br>$t_f$<br>$t_c$ | Off-voltage Rise Time<br>Fall Time<br>Cross-over Time | $V_{DD}$ = 400V, $I_D$ = 60A,<br>$R_G$ = 4.7Ω, $V_{GS}$ = 10V<br>(see test circuit, Figure 5) | | 51<br>46<br>108 | | ns<br>ns<br>ns |

SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (2) | Source-drain Current<br>Source-drain Current (pulsed) | | | | 60<br>240 | A<br>A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 60A, $V_{GS}$ = 0 | | | 1.5 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{rrm}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 60A, di/dt = 100A/µs,<br>$V_{DD}$ = 100 V, $T_j$ = 25°C<br>(see test circuit, Figure 5) | | 532<br>9.9<br>37 | | ns<br>µC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{rrm}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 60A, di/dt = 100A/µs,<br>$V_{DD}$ = 100 V, $T_j$ = 150°C<br>(see test circuit, Figure 5) | | 636<br>13.4<br>42 | | ns<br>µC<br>A |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

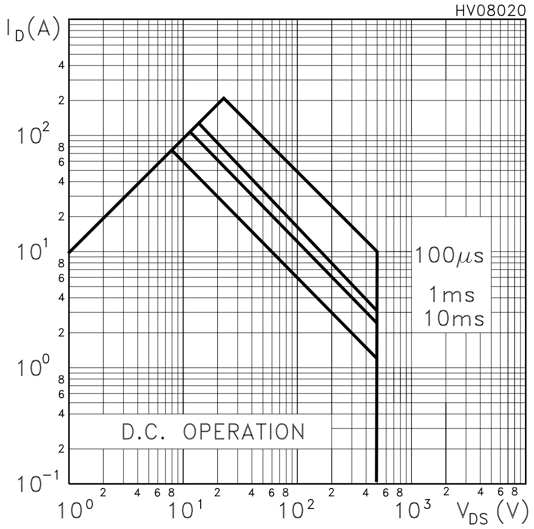
## GATE-SOURCE ZENER DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{GSO}$ | Gate-Source Breakdown Voltage | Igs=± 1mA (Open Drain) | 30 | | | V |

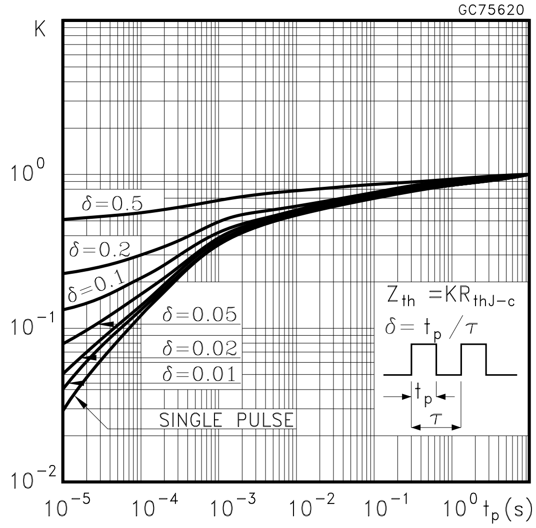
## PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

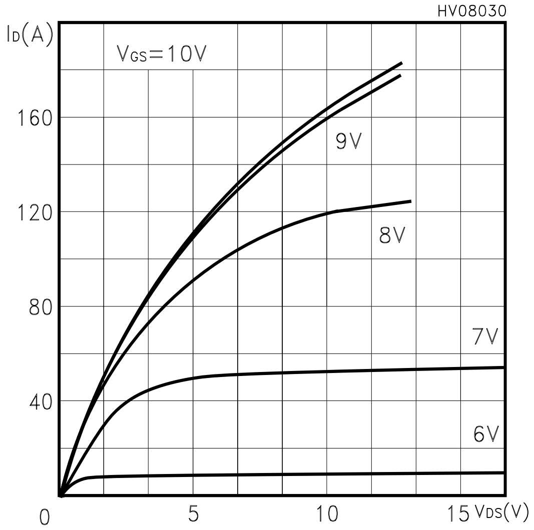
### Safe Operating Area



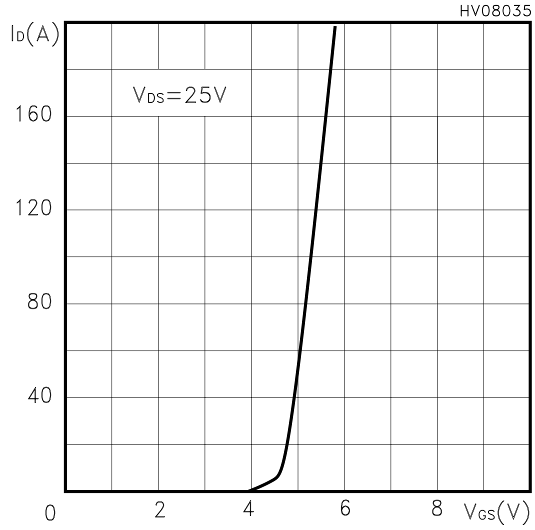

### Thermal Impedance



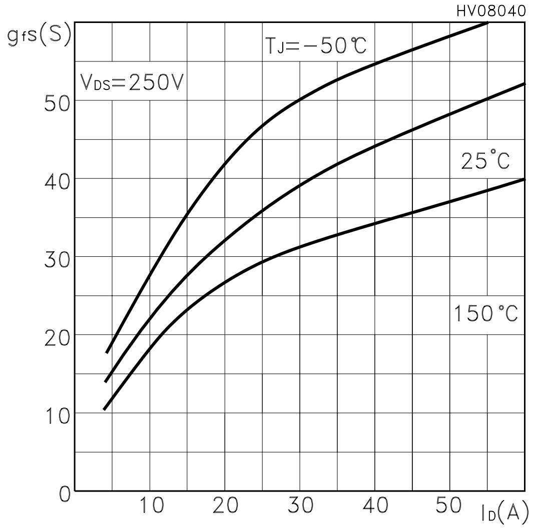

### Output Characteristics



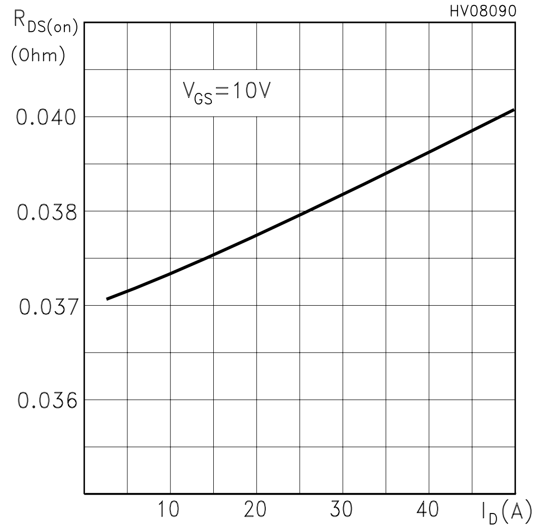

### Transfer Characteristics



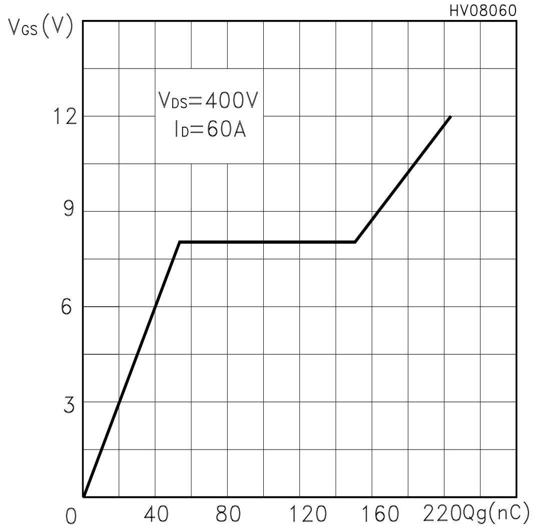

### Transconductance



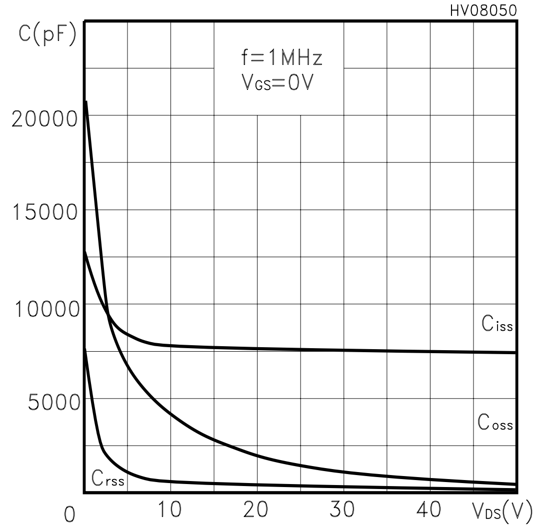

### Static Drain-source On Resistance



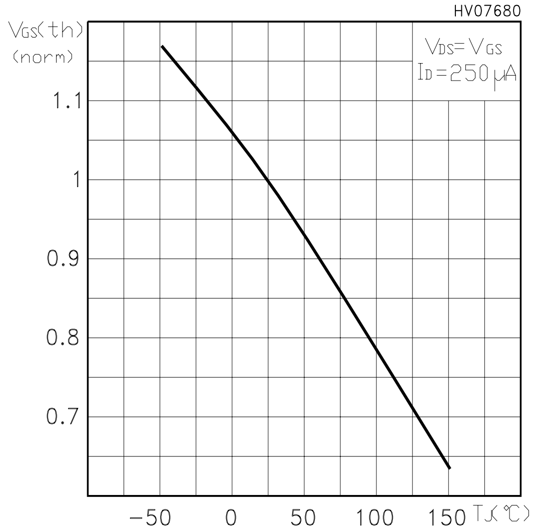
### Gate Charge vs Gate-source Voltage



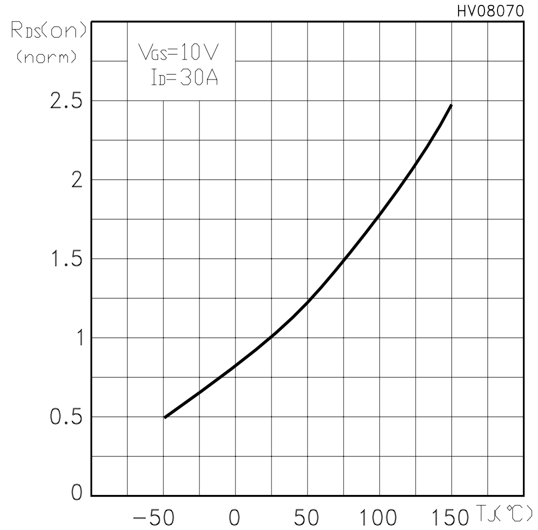

### Capacitance Variations




### Normalized Gate Threshold Voltage vs Temp.




### Normalized On Resistance vs Temperature




### Source-drain Diode Forward Characteristics

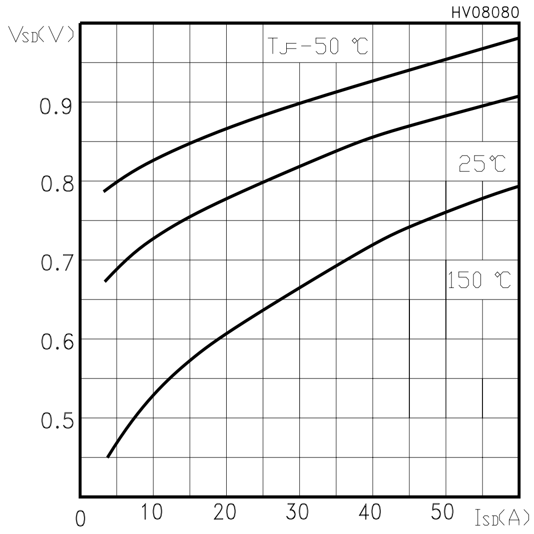


**Fig. 1:** Unclamped Inductive Load Test Circuit

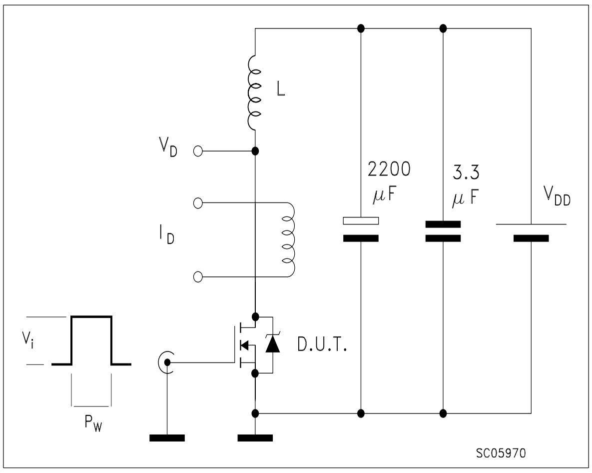



**Fig. 2:** Unclamped Inductive Waveform

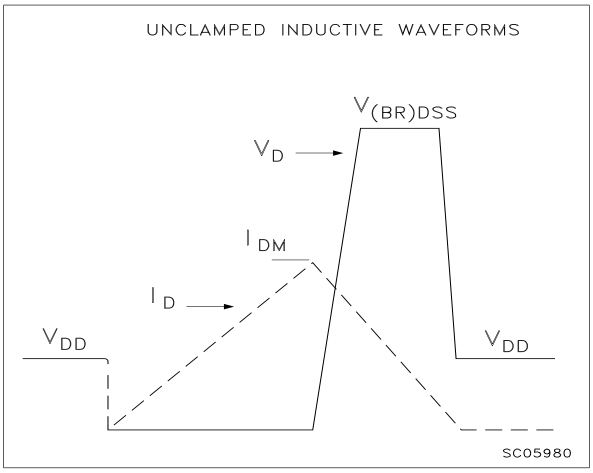



**Fig. 3:** Switching Times Test Circuit For Resistive Load

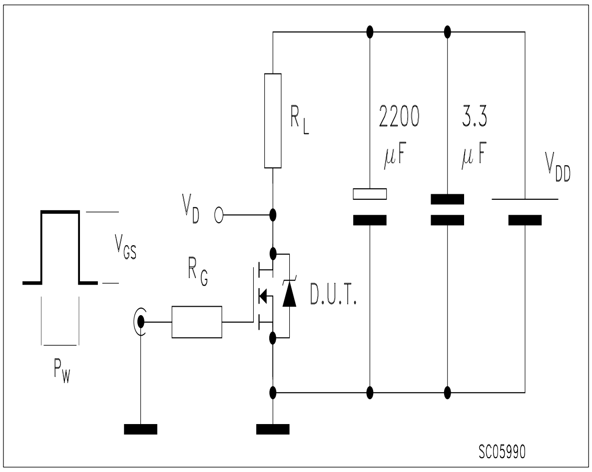



**Fig. 4:** Gate Charge test Circuit

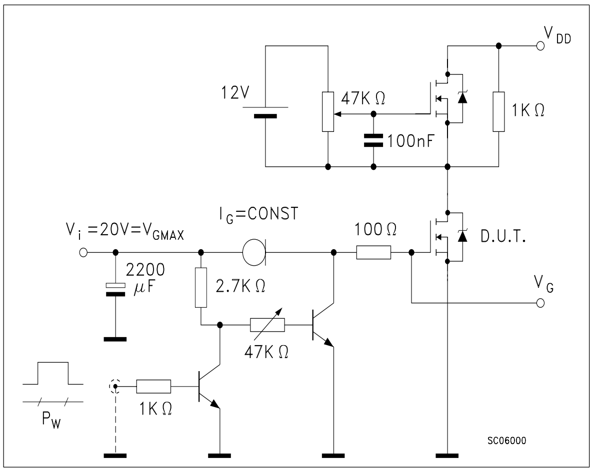
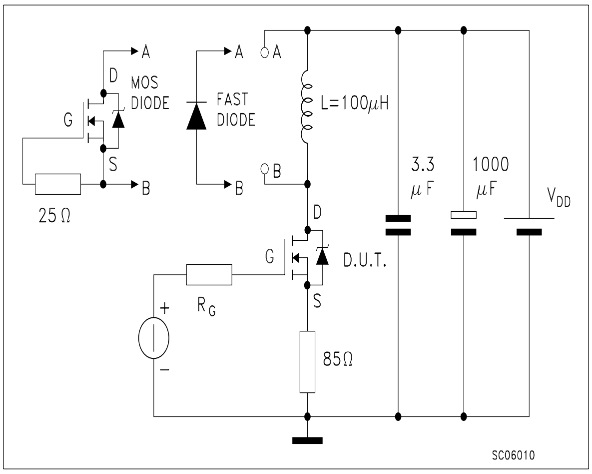



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## ISOTOP MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 11.8 | | 12.2 | 0.466 | | 0.480 |
| B | 8.9 | | 9.1 | 0.350 | | 0.358 |
| C | 1.95 | | 2.05 | 0.076 | | 0.080 |
| D | 0.75 | | 0.85 | 0.029 | | 0.033 |
| E | 12.6 | | 12.8 | 0.496 | | 0.503 |
| F | 25.15 | | 25.5 | 0.990 | | 1.003 |
| G | 31.5 | | 31.7 | 1.240 | | 1.248 |
| H | 4 | | | 0.157 | | |
| J | 4.1 | | 4.3 | 0.161 | | 0.169 |
| K | 14.9 | | 15.1 | 0.586 | | 0.594 |
| L | 30.1 | | 30.3 | 1.185 | | 1.193 |
| M | 37.8 | | 38.2 | 1.488 | | 1.503 |
| N | 4 | | | 0.157 | | |
| O | 7.8 | | 8.2 | 0.307 | | 0.322 |